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Nano-Precision Deep Reactive Ion Etching of Monocrystalline 4H-SiCOI for Bulk Acoustic Wave Resonators with Ultra-low Dissipation

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Integrated mechanical resonators with high quality factors (Q) made in high acoustic velocity materials are essential for a wide range of applications, including chemical sensors, timing resonators, and high-performance inertial sensors for navigation in GPS-occluded environments. While silicon is the most popular substrate for implementation of microelectromechanical systems (MEMS) resonators, SiC exhibits an exceptionally small intrinsic phononic dissipation due to high Akhiezer limits. This paper reports the latest results on nano-precision deep reactive ion etching (DRIE) of monocrystalline 4H SiC-on-Insulator (SiCOI) substrates to explore dissipation limits of bulk acoustic wave (BAW) SiC resonators. We report for the first time on capacitive Lamé mode resonators with $f \cdot Q$ products beyond 1×10^{14} Hz. The contribution of surface roughness to dissipation and practical considerations to etch mirror-polished trenches in SiCOI substrates are discussed, paving the way towards micromechanical SiC resonators with Qs beyond 100 M.

Introduction

Micro- and nano-mechanical resonators are found across a wide range of applications, including consumer electronics, precision robotics, inertial navigation (1 and wearable sensors for health monitoring (2). Critical performance metrics for these resonators include Q and thermo-mechanical Brownian motion noise. Although silicon (Si) is a well-established substrate for high-Q applications, third-generation semi-conductor silicon carbide (SiC) is poised to support small-volume resonators with ultra-high Qs, far beyond the reach of Si. SiC's extraordinary promise of 30-fold improvement in mechanical Q stems from its lower phononic Akhiezer limit relative to Si, approaching that of optical resonators. Recently, our group has shown integrated Lamé resonators with mechanical $f \cdot Q$ figure greater than 1×10^{14} Hz (3), 4-fold beyond the Akhiezer limit of Si and limited by micro-scale surface roughness. This paper presents the challenges in developing a SiC MEMS technology platform for applications with mechanical Qs reaching 100 M.

Multiple barriers hinder the development of SiC MEMS as a technology platform including (a) high development cost of SiC-on-Insulator (SiCOI) substrates (*e.g.,* bare SiC wafer cost, preparation, bonding, and grinding with precise thickness control) and low-volume production, (b) challenges to micromachining of SiCOI substrates at wafer-level and with nano-sale precision, and (c) a limited processing thermal budget. While the cost

of 100 mm n-doped 4H-SiC substrates approaching $850 is an undeniable barrier to the development of thick monocrystalline SiC MEMS, the SiC wafer cost has been steadily decreasing; the trend is expected to continue owing to the growing demand from the booming EV industry. However, the limited deployment base of high-density dry etchers dedicated to SiC wafer-level processing severely obstructs basic research. To wit, there are few papers focused on deep reactive ion etching (DRIE) of SiC (4) and even fewer on DRIE of SiCOI substrates (5) for ultra-high Q MEMS applications (6).

This paper focuses on the challenges in developing a SiC MEMS technology platform for applications requiring ultra-low dissipation. Design consideration and major results of recently published results (3) are briefly recalled here to justify the development of deep reactive ion etching of thick monocrystalline SiCOI substrates with nano-scale precision to fabricate of bulk acoustic wave resonators with ultra-low dissipation.

Design of SiC Lamé Resonators with Ultra-low Dissipation

SiC's pristine material properties conspire to restrict anharmonic phonon-phonon scattering in the Akhiezer regime. All relevant material properties – a low phonon relaxation time ($\tau = 2.2$ ps), a high Debye velocity ($c = 8.8$ km/s), a small Grüneisen parameter ($\gamma = 0.3$), a high density ($\rho = 3.2$ kg/m^3) – contribute to minimize phonon-phonon scattering in SiC, making it an acoustically superior substrate relative to common micro-machinable substrates at wafer level (7,8) (Figure 1). However, adequate designs and pristine fabrication are required to bind dissipation to Akhiezer damping in SiC micromechanical resonators:

$$\frac{1}{Q} = \frac{1}{Q_{AKE}} + \frac{1}{Q_{TED,\,Bulk}} + \frac{1}{Q_{TED,\,Surface}} + \frac{1}{Q_{ANC}} + \frac{1}{Q_{SURF}} + \frac{1}{Q_{AIR}} + \cdots \quad [1.a]$$

where,

$$Q_{AKE} \sim \frac{\rho c^2}{\gamma^2 c_v \tau} \quad [1.b]$$

In equations [1], AKE refers to Akhiezer damping, TED to thermoelastic damping in both the bulk of the material and at its surface due to surface roughness [9], ANC to anchor loss, SURF to surface loss (10), and AIR to viscous damping. Viscous damping is negligible in this work because the devices operate at µTorr vacuum levels. Unlike flexural resonators, BAW resonators can maintain performance in packaged environments with mTorr vacuum levels (11). Surface loss may play a role in the observed degradation of Q-factors of unpackaged SiC resonators over time and is not

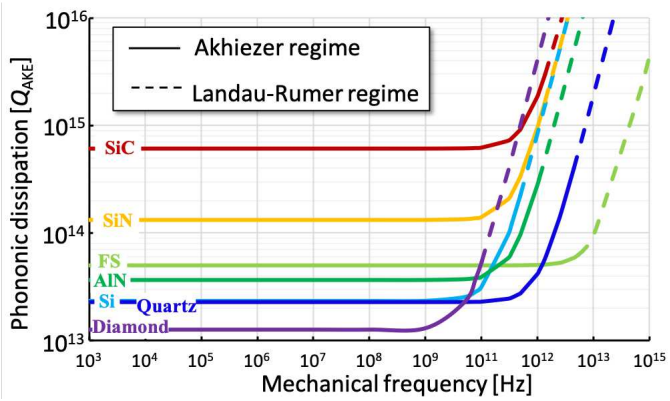

Figure 1. Among micro-machinable substrates, SiC is poised to support ultra-high Q resonators.

discussed in this work.

Thermoelastic Damping in SiC Resonators due to Surface Roughness. A higher thermal conductivity ($\kappa = 370$ W/(m·K)), a higher coefficient of thermal expansion ($\alpha = 4.3$ ppm/°C), and a higher density generate about 10× more TED in SiC than in Si. Fortunately, TED is not only material dependent but also mode and frequency dependent as shown by equation [2].

$$Q_{TED} = \frac{1}{\Psi} \cdot \frac{c_v^2}{\alpha \rho \kappa T} \cdot \frac{1 + (\omega\tau)^2}{\omega\tau} \qquad [2]$$

In equation [2], c_v refers to the specific heat, Ψ to a mode dependent factor, ω to the angular frequency and τ to the time constant of eigenthermal modes (12). The Lorentzian term defines three separate operational regimes: isothermal ($\omega\tau << 1$), Debye peak ($\omega\tau \sim 1$), and adiabatic ($\omega\tau >> 1$) as shown in

Figure . In the first and last regimes, the efficiency of thermomechanical couplings is poor, resulting in higher Q_{TED}. Bulk acoustic wave (BAW) resonators with millimeter-scale in-plane frequency-setting dimensions operate deep in the adiabatic regime. In contrast, TED is exacerbated near the Debye peak where flexural resonators typically operate, making them inadequate to reach ultra-high Qs. Among the BAW resonators, square resonators are ideally poised to circumvent the inferior material properties of SiC relative to TED since their constant-volume Lamé mode exhibit Q_{TED} near 1 Billion (B). The acoustic energy dissipation of perfect square resonators (*e.g.*, no release holes nor tethers), operating near 6.27 MHz, is bound to internal Akhiezer damping with an estimated $Q_{TOTAL} \sim 106$ M. However, displacement in the supporting tethers will generate some TED and limit Q_{TOTAL} ~30-60 M, depending on the tethers' dimensions (Figure 2). Finally, the presence of surface roughness along the device's sidewall will generate surface TED, in addition to bulk TED, and limit $Q_{TOTAL} \sim$ 16-30 M, assuming negligible anchor loss (3). Numerical simulations predict Lamé resonators with 1-unit cell have $Q_{ANC} \sim 47$ M while with 2-unit cells, $Q_{ANC} \sim 9$ B. The predicted Q_{TOTAL} is 17 M for 1-unit cell Lamé and 26 M for 2-unit cells Lamé taking into account Akhiezer damping, bulk and surface TED, and anchor loss altogether. SiC Lamé resonators with quantum-limited dissipation require complete acoustic deafness to the substrate as well mitigating surface thermoelastic damping through deep reactive ion etching with nano-scale RMS surface roughness near 50 nm.

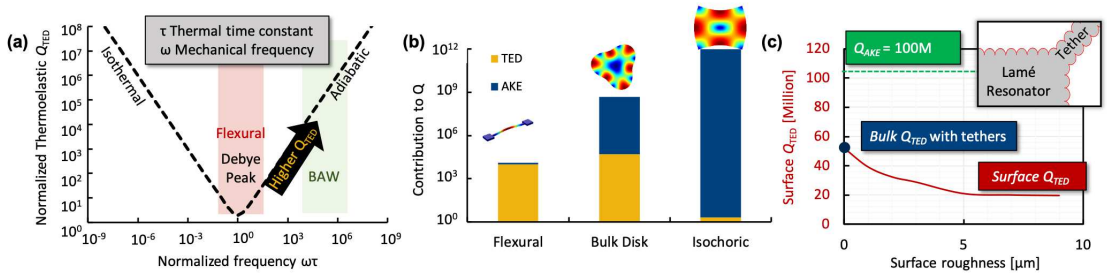

Figure 2. Operating BAW resonators in the adiabatic regime alleviates TED. (a) BAW resonators in the adiabatic regime exhibit higher Q_{TED} relative to flexural resonators operating near the Debye peak (b) In addition to this, constant-volume Lamé modes without tethers almost completely circumvent TED (c) However, Lamé resonators develop TED because of tether strain and roughness.

Nano-precision Deep Reactive Ion Etching of Silicon Carbide on Insulator Substrates

In this section, we describe SiCOI substrate processing and our two-prong approach to nano-precision high-aspect-ratio DRIE of SiCOI substrates using STS AOE Pro. Prior to MEMS processing, we fabricate the 100 mm SiCOI substrates in collaboration with Disco® for edge trimming and grinding as well as Entrepix® and EVG® for polishing and fusion bonding at 400°C respectively. The high development cost and low-volume fabrication of 40 µm-thick SiCOI substrates (Figure 3) coupled with unreliable SiCOI DRIE results prevent us from confidently processing full SiCOI wafers. Instead, the wafers are diced into quarters and each quarter is processed separately, necessitating the use of nickel coated carrier wafers.

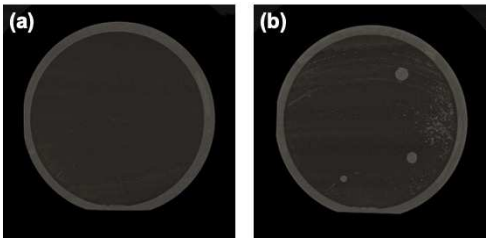

Figure 3. Custom fusion-bonding of 100 mm SiCOI substrates revealing that pressure is necessary (a) during annealing to avoid formation of (b) high-pressure trapped air bubbles. 5 mm edge trimming pre-bonding improves grinding yield.

Figure 4 shows our low-temperature fabrication process flow with a thermal budget constrained by the CTE-mismatch between Si and SiC. Heterogenous SiCOI substrates cannot be annealed at wafer level at temperatures substantially beyond 700°C without severe wafer warping or cracking. However, hour-long annealings at 1,100°C are necessary to densify the BOX and to enable its uniform etching when exposed to HF, rather than being split in two. Likewise, SiC's high work function necessitates the deposition and high temperature annealing of conductive thin films to form an ohmic contact between aluminum wire bonds and SiC. Packaging and other advance processing requiring implementing these steps at wafer level may necessitate the development of homogenous SiCOI substrates (*e.g.,* SiC-on-Insulator-on-SiC) to limit thermal stress. In this work, all high-temperature steps are realized at die level to avoid processing warped SiCOI substrates.

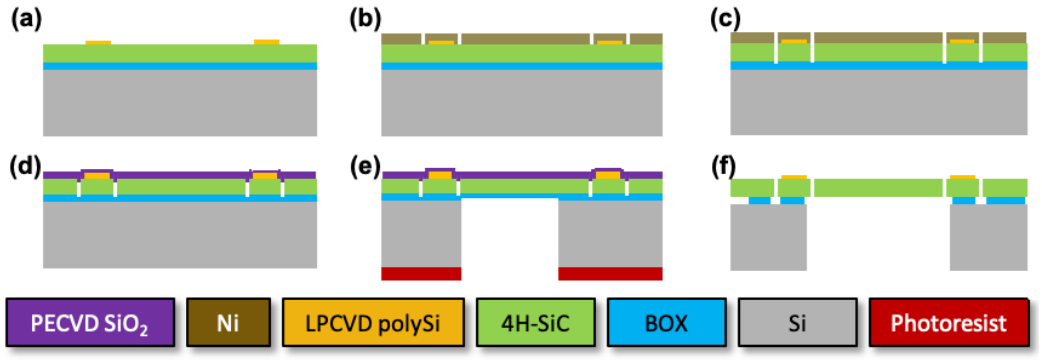

Figure 4. Schematic of monocrystalline SiC micromachining process flow. (a) n-doped LPCVD polycrystalline Si patterning (b) Ni patterning via LIGA process (c) DRIE of SiC (d) PECVD SiO_2 (e) Si cavity (f) Ohmic contact activation via annealing and HF releasing.

We first deposit n-doped LPCVD polycrystalline silicon (polySi) to form an ohmic contact with n-doped 4H-SiC (Figure 4.a). Breaking the strong Si-C bonds requires high self-bias DC voltages leaving photoresist and silicon dioxide (SiO_2) as inadequate mask materials with selectivity near or below 4:1. We use electroplated Ni as a hard mask for the DRIE of SiCOI substrates (Figure 4.b). The benefits of electroplated Ni include low stress relative to other Ni deposition methods, high selectivity to SiC in SF_6 plasma chemistries and vertical and smooth profiles, which is critical to etch SiC with nanoscale precision. Mask tapering, non-uniform Ni electroplating rate and sometimes large thickness variations across wafers practically limit Ni's effective mask selectivity to ~15:1. Low-current dummy electroplating runs are used to remove contamination due to metal dissolution and brightener and additive accumulation while the main run requires high-current density to favor deposition of low-stress Ni. The SiCOI quarter wafers are glued to Ni-coated Si wafers via low melting point crystal bond to facilitate post-etching cleaning. We remove excess crystal bond with a razor blade, to prevent sputtering as well as bubble formation which can degrade thermal contact between the SiCOI quarter and the Ni-coated Si carrier wafer. After dry etching SiC (Figure 4.c), the wafers are cleaned in diluted HNO_3, Piranha, and EKC 265. PECVD SiO_2 layer is deposited to preserve pristine SiC trenches through backside processing (Figures 4.d-e). The SiCOI quarter-wafers are diced, annealed at 1,100°C for 15 hours, annealed at 1,200°C for 4 min in a N_2 environment, and released in HF (Figure 4.f). Annealing at these temperatures is necessary to activate the polySi on SiC ohmic contact; however, N_2 becomes no longer inert and, with flow rates exceeding 0.1 slm, may form SiN with polySi, degrading the SiC electrodes' surface quality.

Although Ni has sufficient selectivity to SiC and can be patterned with high-fidelity,

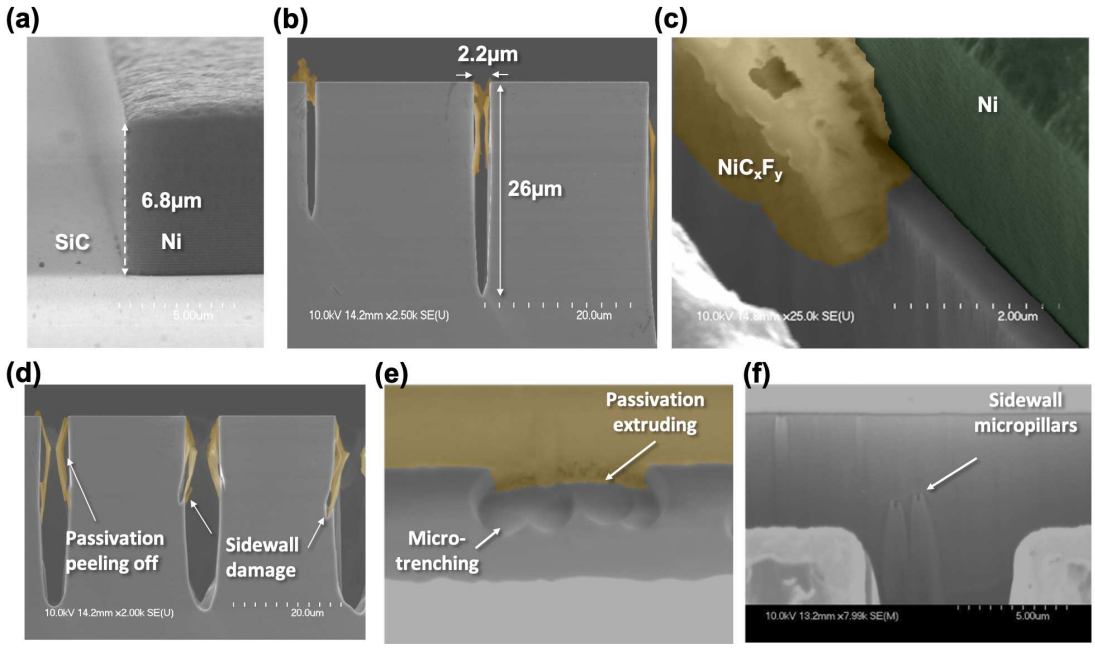

Figure 5. High-aspect-ratio deep reactive ion etching of SiC substrates using low SF_6 recipe (a) High-fidelity Ni mask with vertical and smooth profiles (b) C_xF_y by-products polymerization limits the trench's aspect-ratio (c) the NiC_xF_y deposits on the Ni mask without degradation. (d) sidewall damage due to passivation peeling-off (e) localized microtrenching enables passivation extrusion (f) sidewall micropillars grow and may electrically short the device.

vertical, and smooth sidewalls (Figure 5.a), Ni also poses multiple challenges to the implementation of SiC as platform technology for MEMS (Figures 5.b-c). During etching, sputtered Ni particles polymerize volatile C_xF_y etch by-products. There is no known etch chemistry to remove the metallo-fluorocarbon NiC_xF_y passivation and so this passivation progressively builds up on the chamber's sidewall. Unlike the Bosch process which etches high-aspect-ratio trenches in Si through consecutive etch and passivation cycles while maintaining the chamber in pristine conditions (13), DRIE of SiC is to date a dirty process. The NiC_xF_y passivation is manually removed every ~30 RF hours using Scotch-Brite® and IPA. For safety purposes, manual cleaning is done at room temperature which submits the magnets to temperature cycles that slowly degrade the magnetic flux. In addition to this, o-rings degrade extremely quickly due to the plasma's harsh conditions. Over time, the etching conditions drift and the dry etching recipe has to be continuously optimized in dry etchers that are not designed for the DRIE of SiC (*e.g.,* STS AOE). We have migrated our dry etching recipe to STS AOE Pro which does not use o-rings to clamp the wafer on the chuck and have observed more repeatable etch results relative to STS AOE.

Table 1: High-aspect-ratio SiC dry etching recipes using STS AOE Pro

Parameter	Unit	Low SF_6 Recipe	High SF_6 Recipe
Coil power	W	1,000	1,800
Platen power	W	200	300
Pressure	mTorr	8	8
Temperature	°C	2	20
Maximum duration	min	40	70
4µm wide trench depth in a single run	µm	~18	~54
SF_6 flow rate	sccm	40	250
Ar flow rate	sccm	120	50
O_2 flow rate	sccm	0	25
Self-bias V_{DC}	V	80	125
Ni to SiC selectivity	-	~15:1	~15:1

In addition to degrading the chamber's condition, the NiC_xF_y passivation also introduces a wide range of trench defects (Figures 5.d-f). These defects include trench tapering, sidewall damage, sidewall micropillars and sidewall roughness. A high density of surface defects dissipates acoustic energy via surface thermoelastic losses, dominating other loss mechanisms in this work. Moreover, sidewall micropillars can create electrical shorts and potential imbalance between otherwise isolated regions (*e.g.,* device and electrodes) and render microelectromechanical resonators inoperable.

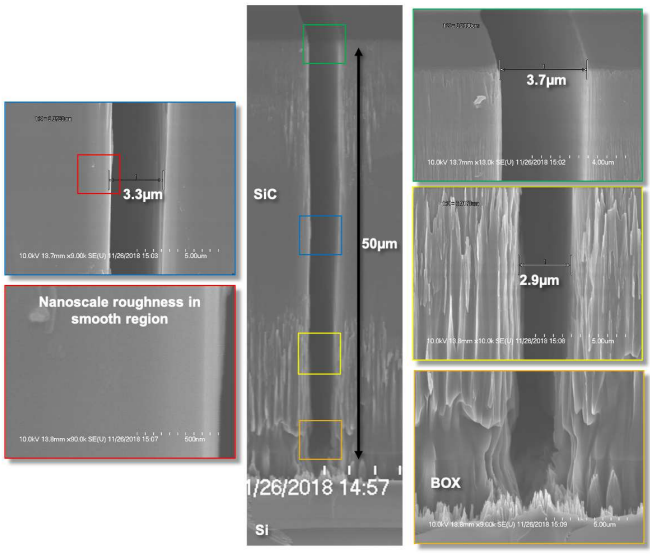

Figure 6. SEM observation of SiCOI trenches etched using low SF_6 recipe in three times with two intermediate *ex-situ* EKC cleaning steps.

We have developed two disparate dry etching recipes to minimize the formation of sidewall micropillars and other

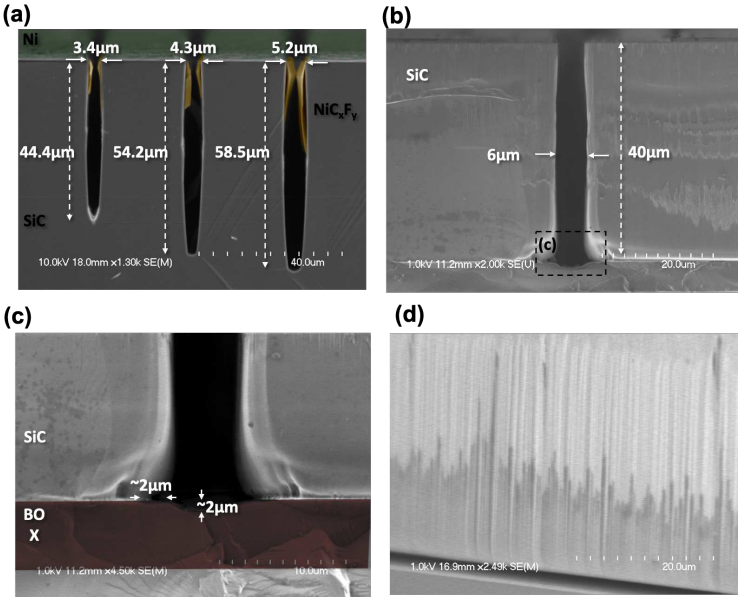

Figure 7. High-aspect-ratio deep reactive ion etching of SiC and SiCOI substrates using the high SF_6 recipe (a) C_xF_y by-products polymerization limits the trench's aspect-ratio. (b) Etching of high-aspect-ratio trenches in SiCOI substrates produces (c) notching near the buried oxide (BOX) layer with (d) smooth and vertical sidewall profiles

etch defects (Table 1). The low SF_6 recipe is designed to minimize the lateral growth rate of the passivation by emphasizing physical etching while the high SF_6 recipe favors chemical etching (Table 1). After 40 RF minutes of low SF_6 recipe, passivation is ~ 400 nm thick. Upon further etching, the passivation thickness will increase beyond 700 nm and peel off. Within 40 minutes, 4 µm wide trenches are 18 µm deep which is insufficient to reach the 40 to 60 µm deep BOX. To prolong the etch, we dissolve the passivation in EKC 162® heated at 80°C in about 2 hours with minimal sonication. At lower EKC temperatures, the passivation is not removed and at higher temperatures, the adhesion of Ni on the seed layer Cr/Au becomes poor, compromising further dry etching. With this approach, we have been able to etch high-aspect-ratio trenches, limited only by the Ni thickness (Figure 6). While, the EKC-cleaned SiC trenches and the Ni mask look pristine, we often observe a much higher density of sidewall micropillars using the low SF_6 recipe, making this recipe unreliable to etch high-aspect-ratio SiCOI trenches with pristine sidewalls and without electrical shorts. All other things constant, continued etching after EKC cleaning generates much more fluorocarbon passivation because more SiC sidewalls are exposed.

Alternatively, the high SF_6 recipe circumvents intermediate *ex-situ* wet cleaning steps by reaching the BOX in a single etch, making it a much more reliable dry etch recipe relative to the low SF_6 recipe. The main challenge associated with the high SF_6 recipe is the ability to etch vertical trenches without bowing as shown in Figure 7. In addition to this, the overall quality of SiCOI trenches is still not as good as in SOIs: the aspect-ratios are limited to below 20:1 and the notch near the buried oxide layer (BOX) is pronounced, which is inadequate for advanced HARPSS-like processes that use sacrificial layers on the sidewall to reach very high aspect ratio capacitive gaps (14).

Capacitive Measurements of Ultra-high *Q* SiC Lamé Mode Resonators

Figures 8.a-b shows a Lamé mode resonator fabricated via DRIE of custom SiCOI substrates. In this section, specific fabrication details related to electrostatic transduction of SiC resonators are discussed prior presenting experimental results. The 6.5 mm × 8 mm SiCOI dies are fixed to PCB boards with transimpedance amplifiers (TIAs) using copper

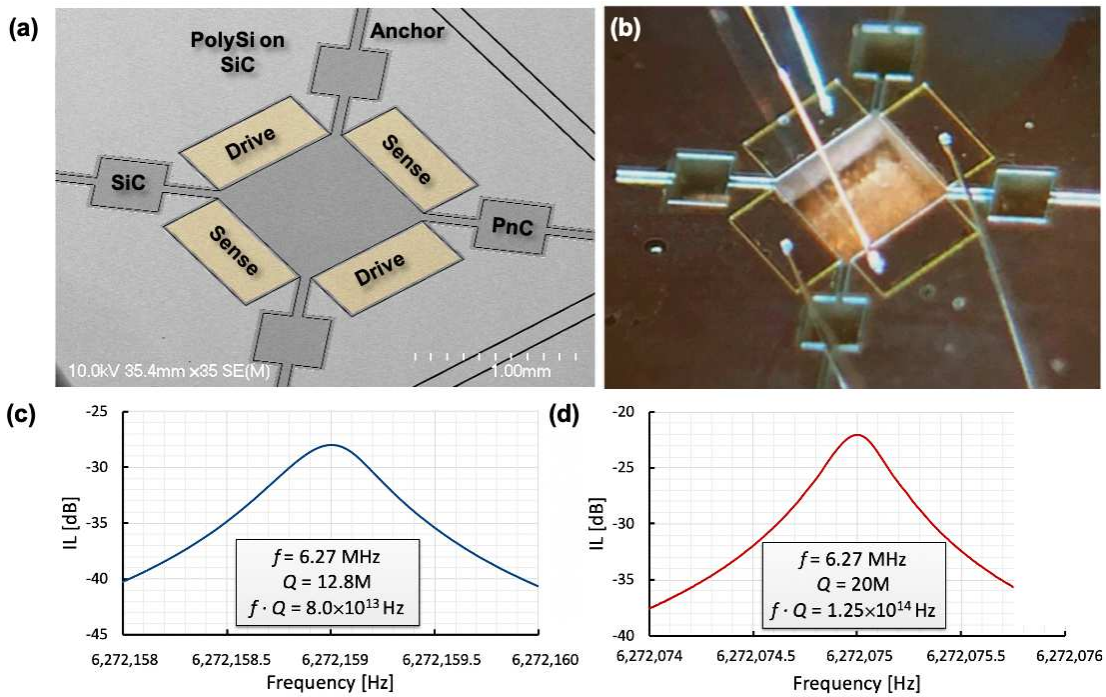

Figure 8. (a) SEM of an ultra-high Q Gen. 2 SiC Lamé resonator fabricated using the low SF_6 recipe (b-c) The Gen. 2 SiC Lamé mode resonators exhibit the highest Qs of 20 M ever reported in Lamé micromechanical resonators as well as break through the barrier of $f \cdot Q = 1\times10^{14}$ Hz, in good agreement with simulations (6).

tape which is observable through the transparent SiC layer and the Si cavity. The 900 µm-wide 6.27 MHz Lamé resonator's frequency characteristics are recorded with a network analyzer that is calibrated to remove feedthrough. Despite 5 µm wide transduction gaps, polarization voltage V_p near 15 V are sufficient to observe clean peaks owing to the resonator's ultra-high Qs in the ten to twenty million range. Drive power is kept near -20 dBm and 30 min of settling time is afforded to the PCB and the device to reach thermal equilibrium. 180° opposite electrodes are shorted on the PCB to capacitively drive and sense the motion of the SiC Lamé resonator.

Figures 8.b-c shows 6.27 MHz Lamé resonators with one PnC unit cell with $Q = 12.8$ M and $f \cdot Q = 8\times10^{13}$ Hz, with a typical Q-factor range between 10 to 12 M. 6.27 MHz Lamé resonators with two PnC unit cells show higher Qs up to 20 M and $f \cdot Q = 1.3\times10^{14}$ Hz. Multiple two-unit cells Lamé resonators of the second design have shown Qs near 15 M. In agreement with simulations, higher Qs are measured in the second design relative to the first. Since additional tether length does not contribute to TED per COMSOL simulations, TED is ruled out to explain the measured discrepancy. We suspect anchor loss to be a dominant loss mechanism for the first design and negligible for the second. Additionally, the measured -12 ppm/°C temperature coefficient of frequency (TCF) of on-axis n-doped 4H-SiC Lamé resonators across -50°C to 85°C is advantageously about 3-fold below that of (100) Si (6).

Discussion

For the first time, capacitive SiC Lamé micromechanical resonators exhibit $f \cdot Q$ products beyond 1×10^{14} Hz in the megahertz frequency range, surpassing performance achieved in previous work (3). To date, SiC mechanical resonators mostly utilize polycrystalline SiC deposited on Si or SiO_2 (15, 16) or operate low-frequency flexural modes near the Debye peak (17), which make them sensitive to both intergranular loss mechanisms and bulk TED, largely negligible in BAW modes in monocrystalline SiC (18).

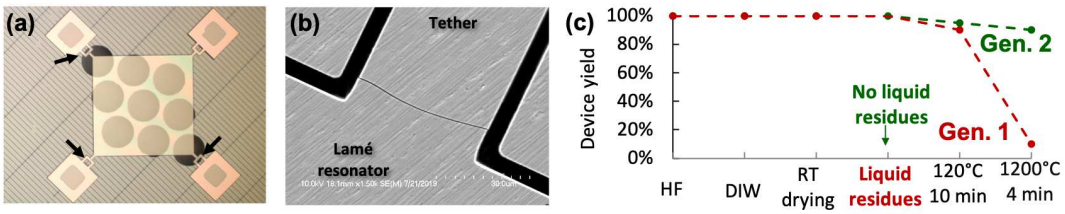

Figure 9. (a) Gen.1 Lamé resonator with Si phononic crystals and (b) cracked tethers which (c) can be avoided by carefully drying the dies, forming Si cavities and increasing tether width

The first generation of SiC Lamé resonators (Gen. 1, Figure 9) had a phononic crystal (PnC) etched through the quarter-wavelength-matched 380 µm thick Si handle layer with an acoustic bandgap centered on the Lamé mode's 6.27 MHz resonant frequency. The design details have been published elsewhere, principally to acoustically isolate center-supported solid disks with Qs up to 18 M at 5 MHz (3). However, this approach did not work well with side supported Lamé resonators. During releasing, almost all devices would present cracks at the junction of the square and one or more of their tethers. Surface tension forces during releasing may have been sufficient to generate or propagate pre-existing cracks, leading to device failure (Figure 9). The second generation of SiC Lamé resonators (Gen. 2, Figure 10) was designed to diminish surface tension forces during releasing and to widen the tethers to improve structural integrity. The width of the tethers is increased to 30 µm and cavities in the Si handle layer are defined below the resonator to remove surface tension forces during releasing. We observed a ~90% yield during releasing; some devices still cracked during Rapid Thermal Annealing (RTA) indicating some initial cracks may be generated during dicing or annealing due to Coefficient of Thermal Expansion (CTE) mismatches between SiC and Si.

Although this paper reports on the highest Q in SiC resonators to date, there is still plenty of room for improvement since a factor near 5× between the theoretical

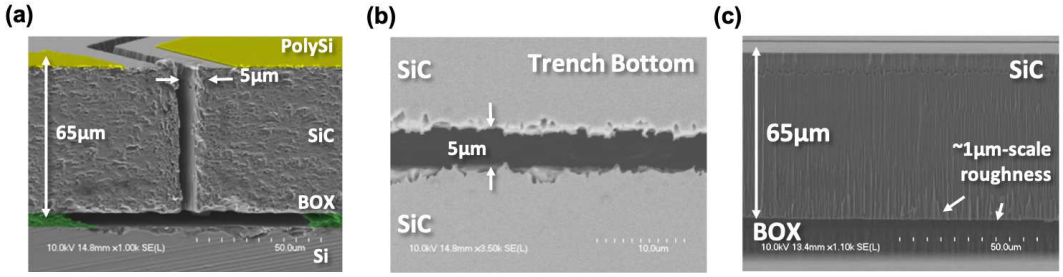

Figure 10. (a) Cross-sectional SEMs of the capacitive transduction gap surrounding the Lamé resonators. (b) Bottom view and (c) side view reveal rough surfaces limiting mechanical Qs.

$f \cdot Q_{AKE}$ = 6.6×10^{14} Hz Akhiezer limit and our highest measured $f \cdot Q_{Meas.}$ = 1.3×10^{14} Hz still remains. We expect to achieve *Q*s near 50 M with Gen. 2 design if surface roughness can be maintained below 50 nm (Figure 10). Complementary studies are required to validate the theoretical value of the Grüneisen parameter γ since the Akhiezer limit of SiC has not yet been observed experimentally. We are currently assuming an isotropic value for γ while it has been demonstrated that γ is anisotropic and that the Akhiezer limit is mode dependent. However, Lamé modes are pure shear and have the lowest γ, near the predicted value assuming isotropic crystals. In contrast, our numerical simulations suggest that chaotic surface roughness generates surface TED which concurs with bulk TED and Akhiezer damping to limit *Q* near 26 M for Lamé resonators with two-unit PnC cells. We observe an excellent agreement between the highest measured *Q* of 20 M and the expected *Q* of 26 M. In fact, outlier Lamé resonators can show *Q*-factors as low as 5 M (Figure 11). We suspect that surface roughness is more pronounced in these outlier resonators. Despite their lower *Q*s, these outlier resonators are acoustically decoupled from the substrate since their dissipation is independent of mounting conditions. Breaking their tethers one by one or suspending the die using tension forces in the wire bonds does not significantly change *Q*.

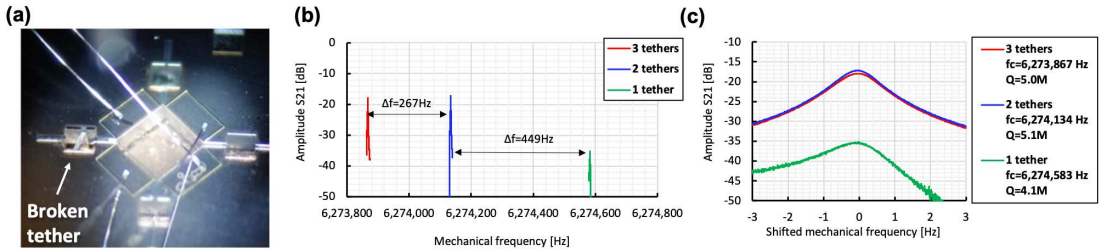

Figure 11. (a-c) Selectively breaking the tethers reveals small residual compressive stress near 50 MPa and tether-independent *Q*s, revealing low *Qs*~5 M are TED limited.

Additionally, we have observed that *Q*-factors tend to degrade over time by approximately 20-30%. Akin to Si, we suspect the formation of native SiO_2, large particles, and stress relaxation to collectively degrade *Q*. The SiC Lamé resonators in this work are not encapsulated in an inert environment. Further studies are required to estimate the long-term drift behavior of dissipation in packaged devices, with tightly controlled and constant environments (19).

Conclusion

The record high $f \cdot Q$ = 1.25×10^{14} Hz measured from electrostatically transduced SiC Lamé mode resonators reveal thick monocrystalline 4H-SiC-on-Insulator (SiCOI) substrates are well-positioned to explore new frontiers in MEMS instruments and sensors, well surpassing Si's intrinsic quantum limit. Thick monocrystalline SiCOI substrates can exhibit *Q*s beyond 100 M if Lamé resonators operating in the low megahertz frequency can be fabricated with nano-scale roughness. While precision DRIE of SiCOI substrates is still undergoing development, SiC BAW technology prototypes reach dissipation limits unachievable by other monocrystalline substrates. The Lamé mode resonators provide an ideal test vehicle for probing fundamental phonon-phonon dissipation limits and the low TCF of -12 ppm/°C offers insight into the SiCOI's suitability as a high performance, versatile platform for myriad sensors and instruments.

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